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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/057,952

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Akio Nakayama

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EXAMINER

DI GRAZIO, JEANNE A

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/057,952

Applicant(s)

NAKAYAMA ET AL.

Examiner

Jeanne A. Di Grazio

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9, 11, 12 and 14-18 is/are pending in the application.
- 4a) Of the above claim(s) 4-7, 14, 15 and 18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 8, 9, 11, 12, 16 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims

Claims 1, 8, 9, 16 and 17 have been amended per Amendment of December 17, 2004. Claims 10 and 13 have been cancelled. Claims 4-7, 14-15 and 18 have been withdrawn per finality of prior requirement for Election / Restriction.

Priority

Priority to Japanese Patent Applications 2001-028982 (Feb. 6, 2001) and 2001-229099 (July 30, 2001) is claimed.

Drawings

The drawings were received on December 17, 2004. These drawings are Figures 18 and 19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 9, 11, 12, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,680,190 (to Michibayashi et al.) in view of United States Patent 5,777,700 (to Kaneko et al.).

As to claims 1 (amended) and 9 (amended), Michibayashi teaches and discloses a liquid crystal display apparatus including the same transparent material in the TFT semiconductor layer and a sub-pixel electrode and has the following structure: transistors disposed at the intersections of gate lines and source lines (Figure 1B, gate electrode 13 and source electrode 15a and TFT 25), pixel electrodes connected with the (drain electrodes of the) transistors (Figure 1A, pixel electrode 23, Col. 4, Lines 65-67, Col. 5, Lines 35-37), opposite electrodes opposite to these pixel electrodes (Figure 1A, counter electrode 24, Col. 4, Lines 62-64), and liquid crystal held

Art Unit: 2871

between said opposite electrode and said pixel electrodes (Figure 1A, liquid crystal 21, Col. 4., Lines 60-63), wherein said pixel electrodes comprise a first pixel electrode and a second pixel electrode disposed in a layer above an insulating film which is itself disposed in a layer above the first pixel electrode, and having a region that does not overlap with the first pixel electrode (Figure 1A: first sub-pixel electrode 23a and second sub-pixel electrode 23b, insulating film 14), and wherein the first pixel electrode and second pixel electrode are electrically connected (with said drain electrode) (Col. 2, Lines 65-67 and Col. 3, Lines 1 and 2, Col. 5, Lines 35-37)(Figure 9, sub-pixel 42an, contact hole 48, and sub-pixel 42bm), and the first pixel electrode applying a first electric field to the liquid crystal, and the second pixel electrode applying a second electric field whose strength is different from the first electric field to the liquid crystal (Col. 6, Lines 26-40).

Michibayashi does not appear to explicitly specify that a ratio of a first voltage applied to the liquid crystal by the first pixel electrode and a second voltage applied to the liquid crystal by the second pixel electrode is 0.5:1.0 to 0.9:1.0.

Kaneko teaches and discloses a liquid crystal display with improved viewing angle dependence (Title, Abstract, entire patent). With reference to Figure 42B, Kaneko illustrates first pixel electrode (94) and second pixel electrode (96) separated by a gate insulation film (98). The gate insulation film has a thickness of 4,000 Angstroms ($=4 \times 10^4$ nm). Kaneko teaches that with the structure of Figure 42B, viewing angle is improved over conventional art (Column 17, Lines 57-60).

According to Applicant's enabling disclosure, the thickness of the insulation film is directly related to the voltage ratio. According to Applicant's enabling disclosure, "[t]he 400 nm

Art Unit: 2871

(of the insulation film thickness) ... corresponds to a 0.9:1.0 voltage ratio and it is preferable that the above mentioned voltage ratio be greater than this.” (Specification at page 31). Furthermore, Applicant’s enabling disclosure states “... sufficient viewing angle improvement effects can be attained when this thickness is greater than about 800 nm.” (Specification at page 30).

Kaneko is therefore evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to optimize and to maximize an insulation film thickness (= voltage ratio) between pixel electrodes for the purpose of improving upon viewing angle as taught in Kaneko.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Michibayashi in view of Kaneko for improving upon viewing angle.

As to claim 11, with reference to Figure 42B, Kaneko illustrates first pixel electrode (94) and second pixel electrode (96) separated by a gate insulation film (98). The gate insulation film has a thickness of 4,000 Angstroms ($=4 \times 10^4$ nm) (Applicant’s “wherein the thickness of said insulating layer is 500 nm or greater.”).

As to claim 12, the pixel electrode is a transparent electrode (Col. 5, Lines 38-53).

As to claims 16 (amended) and 17 (amended), the method steps of manufacturing the liquid crystal display devices as claimed by Applicant would have been rendered obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in light of the devices as taught and disclosed by Michibayashi in view of Kaneko.

Art Unit: 2871

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,680,190 (to Michibayashi et al.) in view of United States Patent 5,777,700 (to Kaneko et al.) and further in view of United States Patent 6,198,516 B1 (to Kim et al.).

As to claim 2, Michibayashi does not appear to explicitly specify a cumulative capacitance for stabilizing the pixel potential during the holding period formed between the second pixel electrode and a storage capacitance electrode line or between the second pixel electrode and the preceding gate line adjacent thereto.

Kim teaches and discloses an LCD having a TFT formed at an intersection of data and capacitor lines (Title, entire patent). Kim has storage capacitance obtained between the storage line and the first pixel electrode and between the gate line and the second pixel electrode (Col. 3, Lines 34-38) so that parasitic capacitance is reduced thereby reducing signal delay and thus fast operation of the LCD device is possible (Col. 3, Lines 39-47).

Kim is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to include the structure of a storage capacitance obtained between the storage line and the first pixel electrode and between the gate line and the second pixel electrode for reduced parasitic capacitance, reduced signal delay, and fast operation of an LCD device.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Michibayashi in view of Kim to reduce parasitic capacitance thereby reducing signal delay and thus fast operation of the LCD device is possible (Col. 3, Lines 39-47).

Art Unit: 2871

As to claim 3, Michibayashi does not appear to explicitly specify that the first pixel electrode is in the same layer as the gate line.

Kim has a first pixel electrode in the same layer as a gate line (Figure 3) for connecting the pixel electrode with the gate electrode, manufacturing ease and efficiency, and reduced process steps.

Kim is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to form a pixel electrode in a same layer as a gate line for connecting the pixel electrode with the gate electrode, manufacturing ease and efficiency, and reduced process steps.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Michibayashi in view of Kim for connecting the pixel electrode with the gate electrode, manufacturing ease and efficiency, and reduced process steps.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,680,190 (to Michibayashi et al.) in view of United States Patent 5,777,700 (to Kaneko et al.) and further in view of United States Patent 6,215,542 B1 (to Lee et al.).

As to claim 8 (amended), Michibayashi does not appear to explicitly specify a second pixel electrode with an opening in the central portion of said second pixel electrode through which an insulating film and liquid crystal are held between the first pixel electrode and opposite electrode in that opening.

Lee teaches and discloses a liquid crystal display with improved viewing angle and transmittance (Title, entire patent). With reference to Figures 4A and 4B, Lee illustrates a pixel electrode (33) with a slit (S2) in the center of the pixel (33). A counter electrode (22) opposes the pixel electrode (33) with slit (S2). Liquid crystal (27) is held between the pixel electrode and counter electrode. Such a structure results in an increased viewing angle (Col. 2, Lines 40-50).

Lee is evidence that ordinary workers in the field of liquid crystals at the time the invention was made would have found the reason, suggestion and motivation to include a second pixel electrode with an opening through which an insulating film and liquid crystal are held between the first pixel electrode and opposite electrode in that opening for increased viewing angle.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Michibayashi in view of Lee for increased viewing angle.

Response to Arguments

Applicant's arguments filed December 17, 2004 have been fully considered but they are not persuasive.

Applicant argues the following points to which the Examiner responds in turn.

(1) "Thus, providing no motivation or suggestion except the above noted quotes from the specification of the Applicants, the outstanding Office Action asserts that one of ordinary skill in the art would modify the device of Michibayashi in view of Kaneko." (Remarks at page 10).

(1) It is respectfully noted, that the Office Action has in fact provided motivation to combine the references as pointed out. Kaneko teaches that with the structure of Figure 42B, **viewing angle is improved over conventional art** (Column 17, Lines 57-60).

(2) “In the present case, the outstanding Office Action identifies no common problem confronting the skilled artisan by which the artisan would have selected certain elements of Kaneko to combine with the device of Michibayashi.” (Remarks at page 10).

(2) It is respectfully noted that this is not correct. **Both** references are drawn to solving the same problem: **improved / wide viewing angle**. Please see Michibayashi for example Column 1, Lines 8-10 “Field of the Invention”). Please see Kaneko (Column 17, Lines 57-60).

(3) “Specifically, Kaneko does not teach or suggest that a thickness of a gate insulating film affects in any way viewing angle.” (Remarks at page 10).

(3) The entire structure collectively of Figure 42 contributes to an improved viewing angle as noted. A skilled artisan interested in improving / widening viewing angle would have gleaned from both references (each drawn to improving / widening viewing angle) that modifications of the disclosed structures would lead to an improved / wider viewing angle than that over the conventional art.

(4) Regarding Applicant’s arguments about impermissible hindsight,

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the

Art Unit: 2871

applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In further response to Applicant's arguments, the Examiner notes that United States Patent 6,335,771 B1 (to Hiraishi) teaches that thickness of a gate insulating film affects threshold voltages applied to TFTs and in turn affects viewing angle (Column 27, Lines 10-36 of the Seventh Embodiment). This has been known to those of ordinary skill in the art since at least 1996.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio
Patent Examiner
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